Triple video output amplifier TDA6103Q

FEATURES

- High bandwidth: 7.5 MHz typical; 60 V (peak-to-peak value)
- High slew rate: 1600 V/µs
- Simple application with a variety of colour decoders
- Only one supply voltage needed
- Internal protection against positive appearing Cathode-Ray Tube (CRT) flashover discharges
- One non-inverting input with a low minimum input voltage of 1 V
- Thermal protection
- Controllable switch-off behaviour.

GENERAL DESCRIPTION

The TDA6103Q includes three video output amplifiers in one single in-line 9-pin medium power (SIL9MP) package SOT111BE, using high-voltage DMOS technology, intended to drive the three cathodes of a colour CRT.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA6103Q	9	DBS9	plastic	SOT111BE

BLOCK DIAGRAM

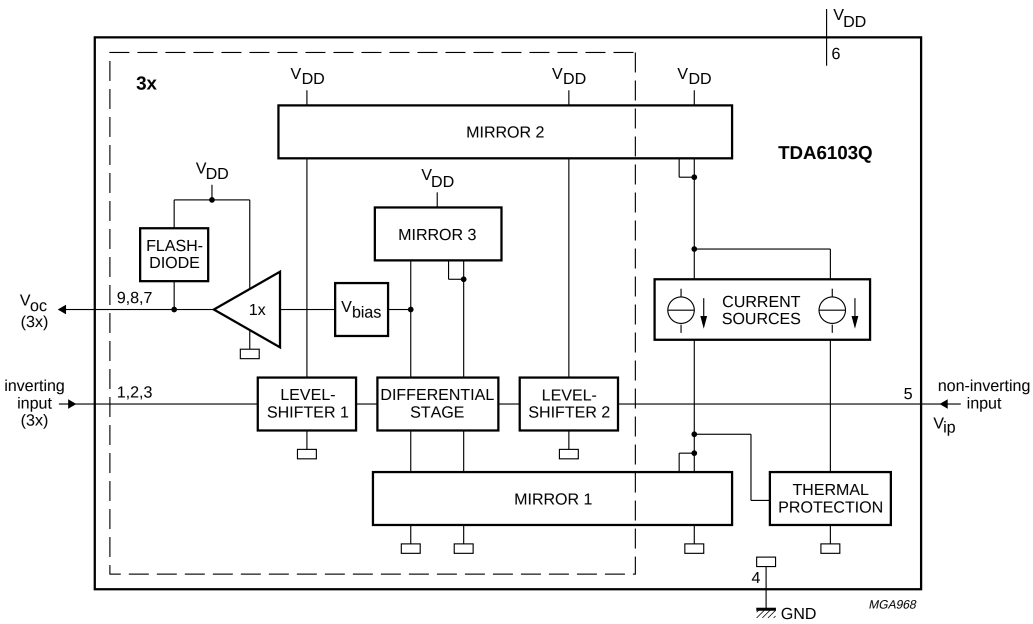


Fig.1 Block diagram (one amplifier shown).

PINNING

SYMBOL	PIN	DESCRIPTION
V_{i1}	1	inverting input 1
V_{i2}	2	inverting input 2
V_{i3}	3	inverting input 3
GND	4	ground, fin
V_{ip}	5	non-inverting input
V_{DD}	6	supply voltage
V_{oc3}	7	cathode output 3
V_{oc2}	8	cathode output 2
V_{oc1}	9	cathode output 1

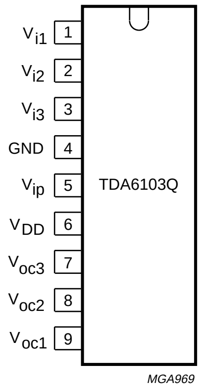


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages measured with respect to GND (pin 4); currents as specified in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		0	250	V
V_i	input voltage		0	12	V
V_{idm}	differential mode input voltage		–6	+6	V
V_{oc}	cathode output voltage		0	V_{DD}	V
I_{ocsmL}	LOW non-repetitive peak cathode output current	flashover discharge = 50 μC	0	5	A
I_{ocsmH}	HIGH non-repetitive peak cathode output current	flashover discharge = 100 nC	0	10	A
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–20	+150	°C
V_{es}	electrostatic handling				
	human body model (HBM)		–	tbf	V
	machine model (MM)		–	tbf	V

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *“Handling MOS Devices”*).

QUALITY SPECIFICATION

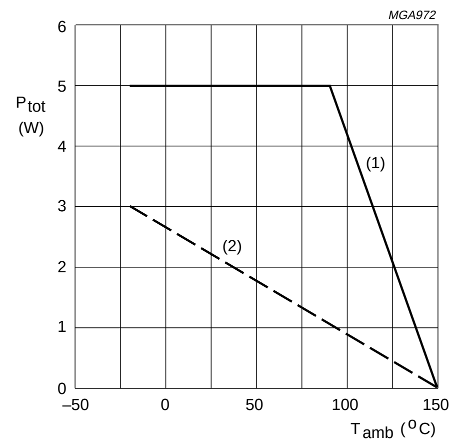
Quality specification *“SNW-FQ-611 part E”* is applicable and can be found in the *“Quality reference pocketbook”* (ordering number 9398 510 34011).

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}fin}$	from junction to fin; note 1	11 K/W
$R_{th\ h\text{-}a}$	from heatsink to ambient	18 K/W

Note

1. An external heatsink is necessary.



(1) Infinite heatsink.
(2) No heatsink.

Fig.3 Power derating curves.

Thermal protection

The internal thermal protection circuit gives a decrease of the slew rate at high temperatures: 10% decrease at 130 °C and 30% decrease at 145 °C (typical values on the spot of the thermal protection circuit).

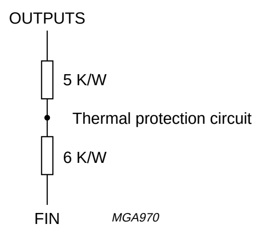


Fig.4 Equivalent thermal resistance network.

CHARACTERISTICS

Operating range: T_j = –20 to 150 °C; V_{DD} = 180 to 210 V; V_{ip} = 1 to 4 V.

Test conditions (unless otherwise specified): T_{amb} = 25 °C; V_{DD} = 200 V; V_{ip} = 1.3 V; $V_{oc1} = V_{oc2} = V_{oc3} = \frac{1}{2}V_{DD}$; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); $R_{th\ h\text{-}a}$ = 18 K/W; measured in test circuit Fig.5.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	quiescent supply current		7.0	9.25	11.5	mA
I_{bias}	input bias current inverting inputs (pins 1, 2 and 3)		–5	–1	+1	μA
I_{bias}	input bias current non-inverting input (pin 5)		–15	–3	+1	μA
$V_{i(offset)}$	input offset voltage (pins 1, 2 and 3)		–50	–	+50	mV
$\Delta V_{i(offset)}$	differential input offset voltage temperature drift between pins 1 and 5; 2 and 5; 3 and 5		–	tbf	–	mV/K
C_{icm}	common-mode input capacitance (pins 1, 2 and 3)		–	5	–	pF
C_{icm}	common-mode input capacitance (pin 5)		–	10	–	pF
C_{idm}	differential mode input capacitance between 1 and 5; 2 and 5; 3 and 5		–	1	–	pF
$V_{oc(min)}$	minimum output voltage (pins 7, 8 and 9)	$V_{1-5} = V_{2-5} = V_{3-5} = -1$ V	–	5	10	V
$V_{oc(max)}$	maximum output voltage (pins 7, 8 and 9)	$V_{1-5} = V_{2-5} = V_{3-5} = 1$ V; note 1	$V_{DD} - 10$	$V_{DD} - 6$	–	V
GB	gain-bandwidth product of open-loop gain: $V_{oc1,\ 2,\ 3} / V_{i1\text{-}5,\ 2\text{-}5,\ 3\text{-}5}$	f = 500 kHz	–	0.75	–	GHz
B_S	small signal bandwidth (pins 7, 8 and 9)	$V_{oc(p\text{-}p)}$ = 60 V	6	7.5	–	MHz
B_L	large signal bandwidth (pins 7, 8 and 9)	$V_{oc(p\text{-}p)}$ = 100 V	5	7	–	MHz
t_{pd}	cathode output propagation delay time 50% input to 50% output (pins 7, 8 and 9)	$V_{oc(p\text{-}p)}$ = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 7 and 8	–	38	–	ns
Δt_p	difference in cathode output propagation time 50% input to 50% output (pins 7 and 8, 7 and 9 and 8 and 9)	$V_{oc(p\text{-}p)}$ = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3)	–10	0	+10	ns
t_r	cathode output rise time 10% output to 90% output (pins 7, 8 and 9)	V_{oc} = 50 to 150 V square wave; f < 1 MHz; t_f = 40 ns (pins 1, 2 and 3); see Fig.7	48	60	73	ns
t_f	cathode output fall time 90% output to 10% output (pins 7, 8 and 9)	V_o = 150 to 50 V square wave; f < 1 MHz; t_r = 40 ns (pins 1, 2 and 3); see Fig.8	48	60	73	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_s	settling time 50% input to (99% < output < 101%)	$V_{oc(p-p)}$ = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 7 and 8	–	–	350	ns
SR	slew rate between 50 V to (V_{DD} – 50 V); (pins 7, 8 and 9)	$V_{1-5} = V_{2-5} = V_{3-5}$ = 2 V square wave (p-p); f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3)	–	1600	–	V/µs
O_v	cathode output voltage overshoot (pins 7, 8 and 9)	$V_{oc(p-p)}$ = 100 V square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 7 and 8	–	5	–	%
SVRR	supply voltage rejection ratio	f < 50 kHz; note 2	–	70	–	dB

Notes

1. See also Fig.6 for the typical low-frequency response of V_i to V_{oc}.
2. The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

Cathode output

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 50 µC.

The cathode is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.

The DC voltage of V_{DD} (pin 6) must be within the operating range of 180 to 210 V during the peak currents.

Flashover protection

The TDA6103Q incorporates protection diodes against CRT flashover discharges that clamp the cathode output voltage up to a maximum of $V_{DD} + V_{diode}$. To limit the diode current, an external 1.5 kΩ carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed (for this resistor-value, the CRT has to be connected to the main PCB). This addition produces an increase in the rise- and fall times of approximately 5 ns and a decrease in the overshoot of approximately 3%.

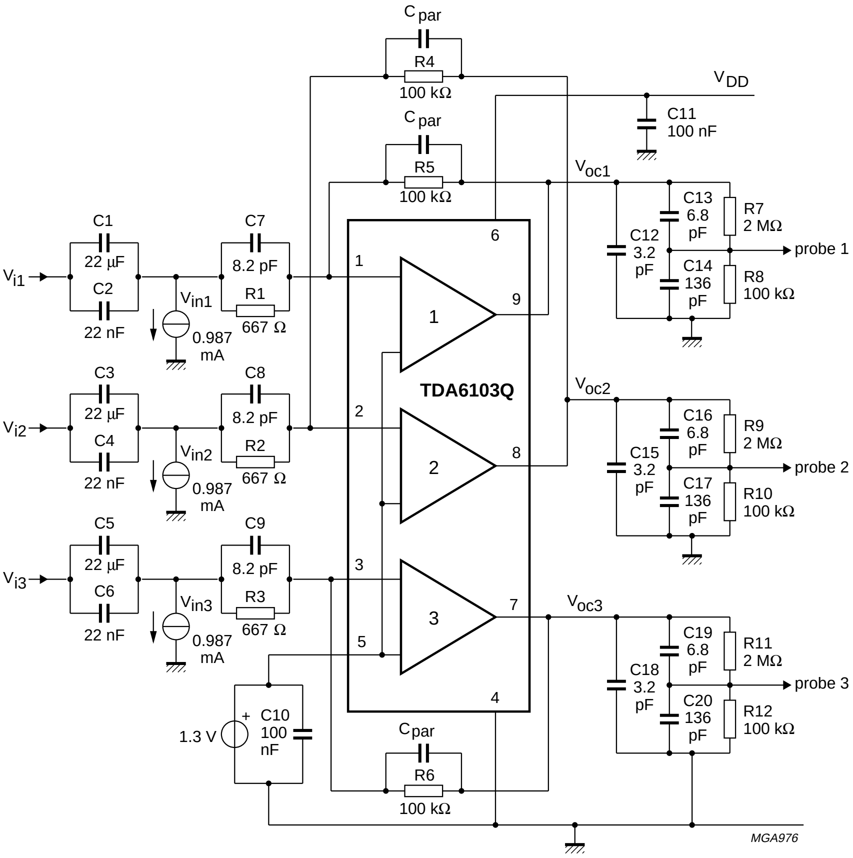
V_{DD} to GND must be decoupled:

1. With a capacitor >20 nF with good HF behaviour (e.g. foil). This capacitance must be placed as close as possible to pins 6 and 4, but definitely within 5 mm.
2. With a capacitor >10 µF on the picture tube base print.

Switch-off behaviour

The switch-off behaviour of the TDA6103Q is controllable. This is due to the fact that the output pins of the TDA6103Q are still under control of the input pins for relative low-power supply voltages (approximately 30 V and higher).

Test circuit



C_{par} = 70 fF.

Fig.5 Test circuit with feedback factor $^{1}/_{150}$.

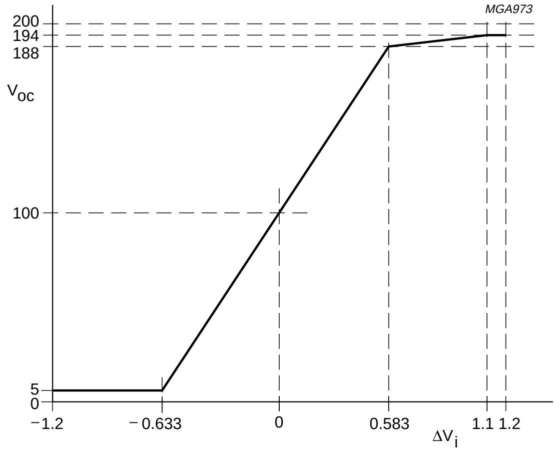


Fig.6 Typical low-frequency (f < 1 MHz) response of $\Delta V_{i1,\,2,3}$ to $V_{oc1,\,2,3}$.

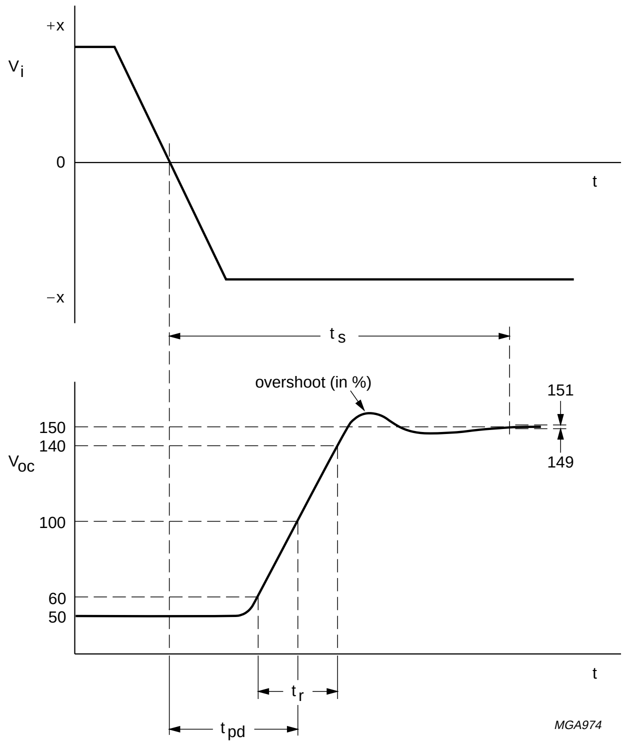


Fig.7 Output voltage (pins 7, 8 and 9) rising edge as a function of the AC input signal.

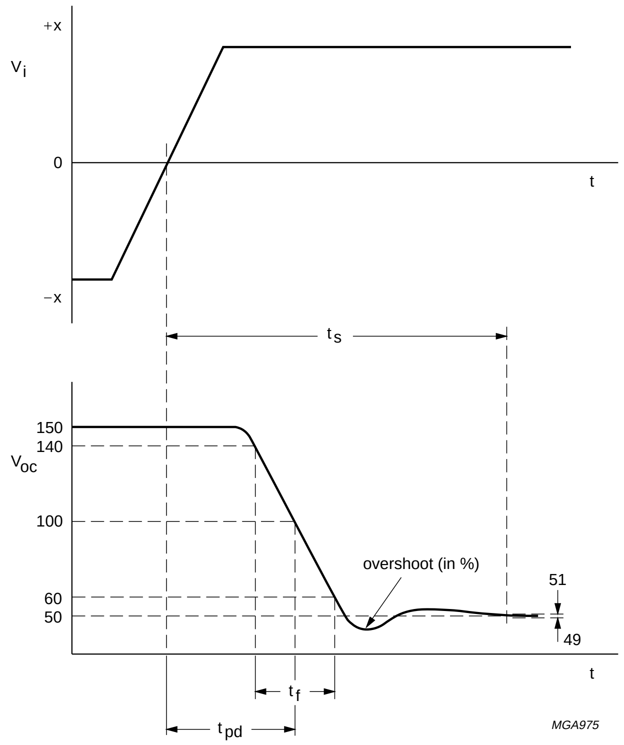


Fig.8 Output voltage (pins 7, 8 and 9) falling edge as a function of the AC input signal.

TEST AND APPLICATION INFORMATION

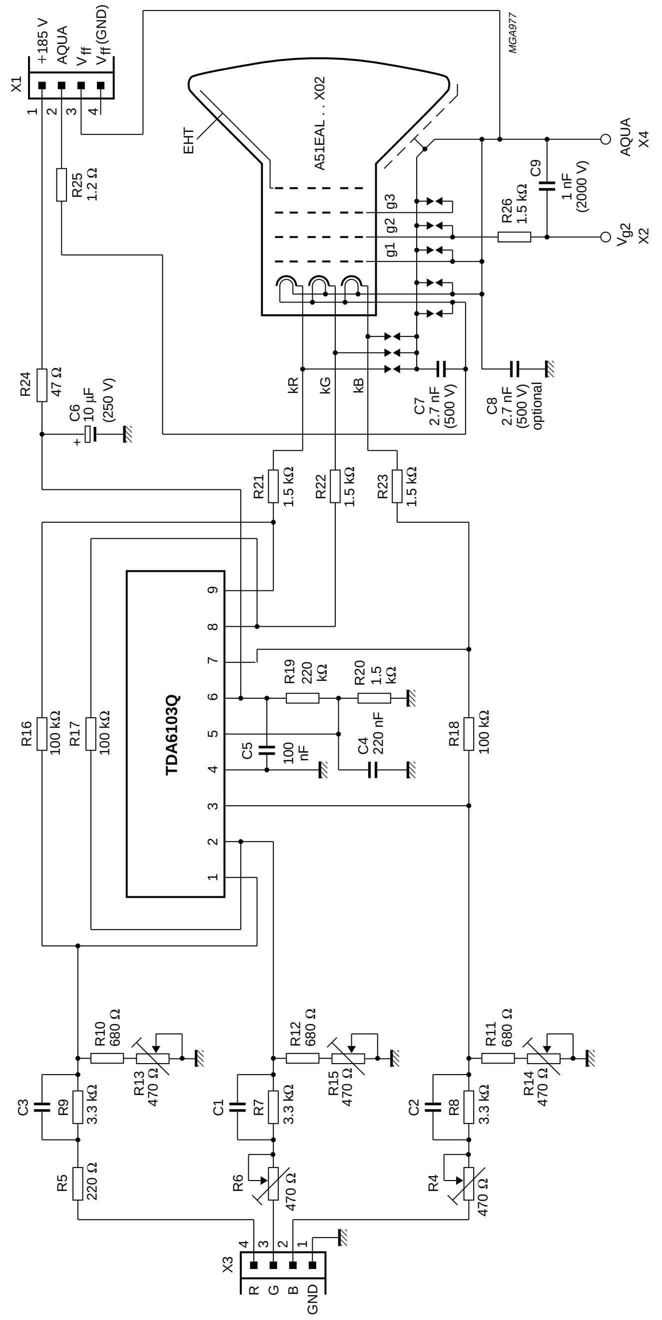
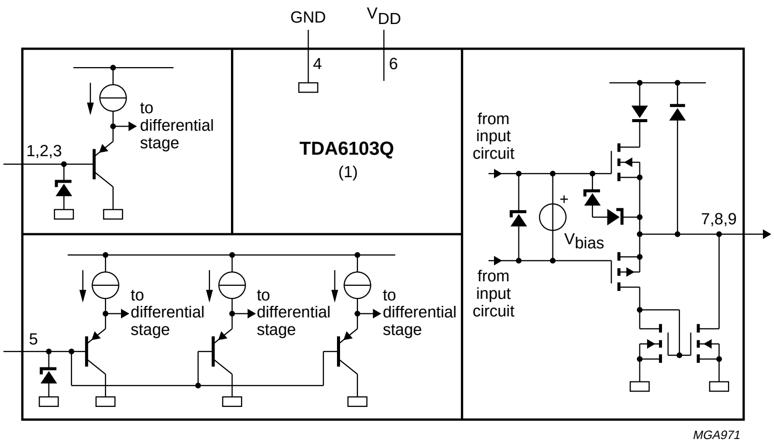


Fig.9 Application diagram.



(1) All pins have an energy protection for positive or negative overstress situations.

Fig.10 Internal pin configuration.

Dissipation

Regarding dissipation, distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6103Q is due to voltage supply currents and load currents in the feedback network and CRT.

The static dissipation equals:

$P_{stat} = V_{DD} \times I_{DD} - 3 \times V_{oc} \times (V_{oc}/R_{fb} - I_{OC})$

R_{fb} = value of feedback resistor.

I_{OC} = DC-value of cathode current.

The dynamic dissipation equals:

$P_{dyn} = 3 \times V_{DD} \times (C_L + C_{fb} + C_{int}) \times f_i \times V_{o(p-p)} \times \delta$

C_L = load capacitance.

C_{fb} = feedback capacitance.

C_{int} = internal load capacitance (≈4 pF).

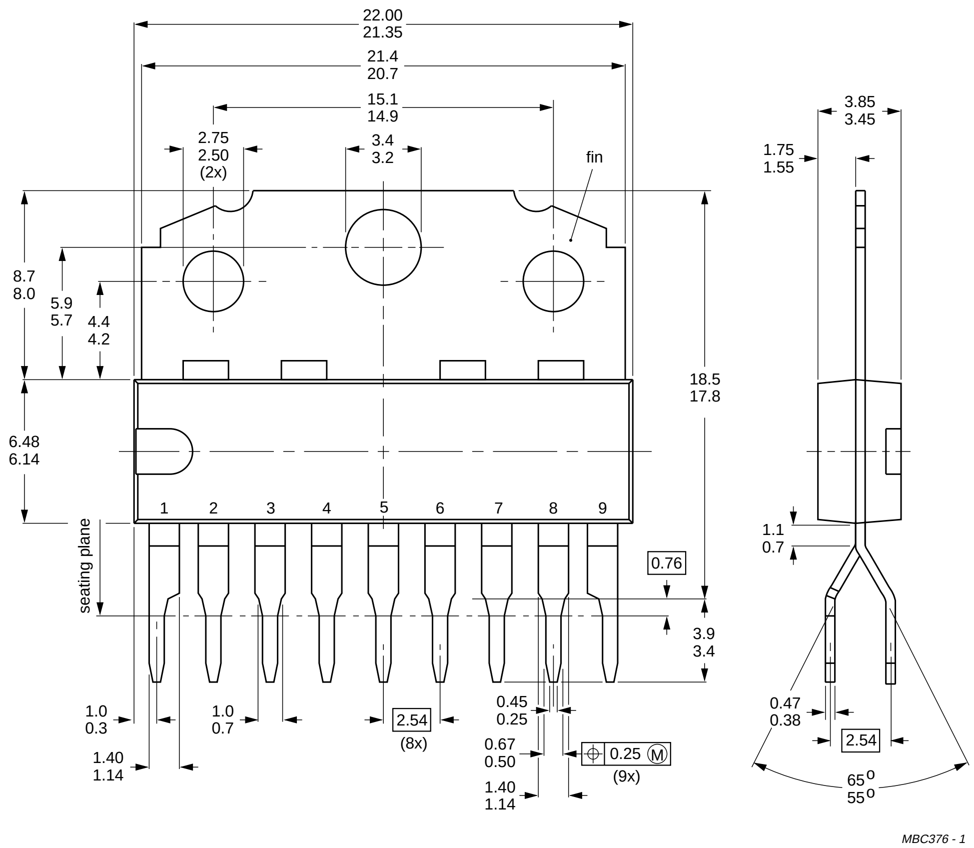
f_i = input frequency.

$V_{o(p-p)}$ = output voltage (peak-to-peak value).

δ = non-blanking duty-cycle.

The IC must be mounted on the picture tube base print to minimize the load capacitance (C_L).

PACKAGE OUTLINE



Dimensions in mm.

Fig.11 Plastic SIL-bent-to-DIL, medium power with fin, 9-pin (SOT111BE).

SOLDERING

Plastic single in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.